LGR-5320 Series

Stand-Alone, High-Speed, Analog and Digital I/O Data Loggers

User's Guide

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October 2013

MEASUREMENT COMPUTING™

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing LGR-5320 Series data acquisition and data logging devices and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text — **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text — *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about LGR-5320 Series hardware is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation by phone, fax, or email with specific questions.

- Knowledgebase: kb.mccdaq.com
- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Introducing the LGR-5320 Series

The LGR-5320 Series includes the following devices:

- LGR-5325
- LGR-5327
- LGR-5329

LGR-5320 Series devices are USB 2.0 full-speed devices supported under Microsoft Windows 7/Vista/XP (32-bit or 64-bit). LGR-5320 Series devices are compatible with both USB 1.1 and USB 2.0 ports.

Each LGR-5320 Series device provides the following features:

- a multiplexed 16-bit A/D converter
- 16 single-ended (SE) or eight differential (DIFF) analog input channels
- 16 digital input connections
- screw terminals for field wiring connections

The LGR-5325 has a maximum sampling rate of 100 kS/s and software-selectable analog input ranges of ±10 V, ±5 V, and ±1 V for all analog input channels. The LGR-5327 and LGR-5329 each has a maximum sampling rate of 200 kS/s and software-selectable analog input ranges of ±30 V ±10 V, ±5 V, and ±1 V for all analog input channels.

The LGR-5329 provides 16 isolated digital input connections including PLC thresholds with 30 V tolerance, and 500 V of isolation between the digital inputs and the host computer, analog inputs, and counter inputs. The LGR-5325 and LGR-5327 provide 16 digital input connections including TTL thresholds with 28 V tolerance. You can configure the DIO connections on all LGR-5320 Series devices to detect and log events based on change of state or pattern recognition.

LGR-5320 Series devices have a single digital alarm output that is implemented as a single Form C relay. You can configure the relay to energize when the trigger condition is met and data is being recorded.

Each LGR-5320 Series device has four counter channels that support the following counter modes:

- Counter (general event counting)
- Period counting
- Pulse width counting
- Edge-to-edge timing
- Up/down counting

The LGR-5327 and LGR-5329 counter channels also support 1X, 2X, and 4X encoder counting. You can configure each encoder counter channel for single-ended or differential mode using an external switch.

LGR-5320 Series devices save data to and retrieve data from a Secure Digital (SD) or Secure Digital High Capacity (SDHC) memory card. All devices require 9 VDC to 30 VDC of external power.

Connect all signals to the screw terminals.

Functional block diagram

LGR-5320 Series functions are illustrated in Figure 1.

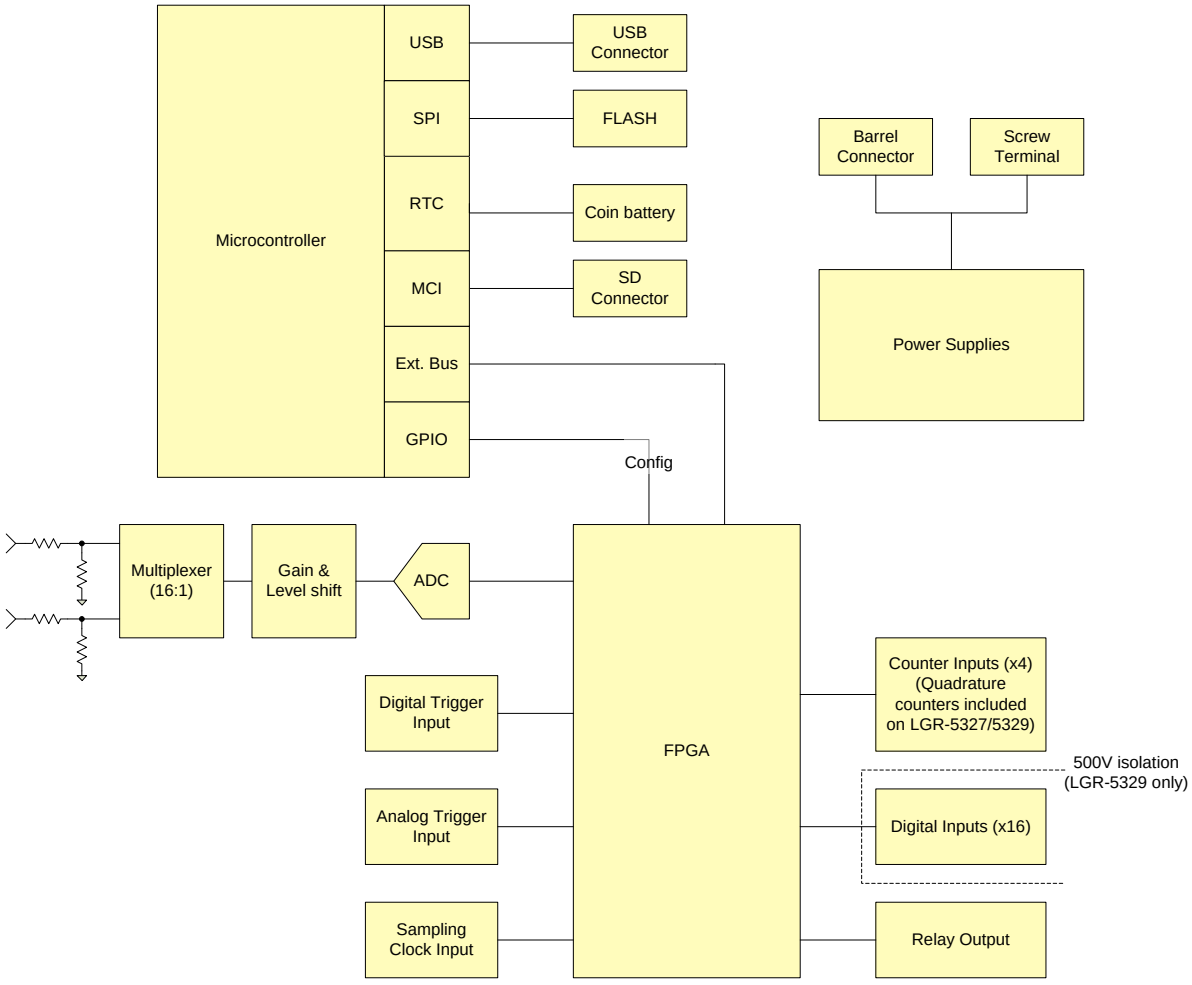


Figure 1. LGR-5320 Series functional block diagram

Installing a LGR-5320 Series Device

What comes with your shipment?

Verify that the following hardware components are included in the shipment:

Hardware

- LGR-5320 Series device – LGR-5325, LGR-5327, or LGR-5329
- USB cable (2-meter length)
- SD card
- 9 VDC, 1 A external power supply for use when LGR-5320 Series is not powered through the screw terminals

Software

DAQLog CD

Optional components

ACC-202 Din-rail kit

Accessory for mounting a LGR-5320 Series device to a standard DIN rail. Use the thread-forming screws to attach the DIN rail clip to your device.

Documentation

In addition to this hardware user's guide, a *DAQLog Quick Start* is included with the LGR-5320 Series shipment. This booklet provides instructions about installing the software and logging data.

Unpacking

As with any electronic device, take care while handling to avoid damage from static electricity. Before removing the LGR-5320 Series device from its packaging, ground yourself using a wrist strap or touch either the computer chassis or other grounded object to eliminate any stored static charge.

If the device is damaged, notify Measurement Computing Corporation immediately by phone, fax, or email.

- Knowledgebase: kb.mccdaq.com
- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

For international customers, contact your local distributor. Refer to the International Distributors section on our web site at www.mccdaq.com/International.

Installing the software

Refer to the *DAQLog Quick Start* for instructions on installing and using the DAQLog software.

Installing the device

When you install a LGR-5320 Series device, you can set it up to operate in one of the following modes:

- *USB* mode—The device is connected to a USB port on your host computer, and controlled by USB command. Use this mode to configure and load logger settings to a logger using DAQLog software.
- *Logging* mode—The device has no active USB connection, all buttons on the logger are enabled, and the device can read from or write to an installed SD card. Use this mode to load configuration settings and log data using LGR-5320 Series logger features.

LGR-5320 Series logger operation modes are illustrated in Figure 2.

Figure 2. LGR-5320 Series USB mode/logging mode state diagram

Setting up a device in USB mode

Complete the following steps to set up a LGR-5320 Series device in USB mode:

1. Connect the 9 VDC, 1 A external power supply to the external power connector (see Figure 4 on page 12), and plug the adapter into an electrical outlet. [1]
2. If the device is configured for **Autostart new log upon device powerup** in DAQLog, press the Start button on the device to stop logging before connecting the USB cable to your computer.
3. Turn the computer on, and connect a USB cable from the USB connector on the device (see Figure 4 on page 12) to either a USB port on the computer or an external USB hub connected to the computer.
4. When you connect a LGR-5320 Series device for the first time, a **Found New Hardware** message opens as the device is detected. When the message closes, the installation is complete.

In USB mode, the buttons on the logger are disabled, and the device cannot read from or write to an installed SD card. Access to the SD card can only be made over the USB connection.

Use DAQLog software to configure the device directly or to create a file with device configuration settings. Refer to the *DAQLog Help* and *DAQLog Software User's Guide* for instruction about using DAQLog to configure a LGR-5320 Series device.

Setting up a device in Logging mode

Complete the following steps to set up a LGR-5320 Series device in Logging mode:

1. Insert the SD card with the settings file into the card slot on the device, and disconnect the USB cable from the device.
2. Either connect the device to an electrical outlet (refer to step 1 under *Setting up a device in USB mode* above), or connect the PWR+ terminal to the positive lead of your power source, and the PWR– terminal to the negative lead of the power source. Use a power source that meets the power specifications of the LGR-5320 Series.
3. Connect the LGR-5320 Series device screw terminals to their signal source.
4. Press LOAD on the device to load the settings file to the device if required.
5. Press START on the device to begin logging data.
6. When the LOG LED turns off, the device is done logging.

Replacing the internal 3 V lithium cell battery

LGR-5320 Series devices include a 3 V lithium cell battery that retains the real-time clock value when the device is powered off. If you get incorrect year readings from a device, you may need to replace this battery.

Caution! The discharge of static electricity can damage some electronic components. Before removing the LGR-5320 Series device from its housing, ground yourself using a wrist strap or touch the computer chassis or other grounded object to eliminate any stored static charge.

Complete the following steps to replace the internal 3 V lithium cell battery in a LGR-5320 Series device:

1. Turn the device over and rest the top of the housing on a flat, stable surface.
2. Remove the five screws from the bottom of the device.
3. Hold both the top and bottom sections together, turn the device over and rest it on the surface, and then carefully remove the top section of the case to expose the circuit board.
4. Lift the clip holding the cell battery in the battery compartment and remove the old battery from the compartment.

[1] Providing power to a LGR-5320 Series device before connecting its USB cable to the computer allows the device to inform the host computer (when the USB cable is connected) that the device requires minimal power from the USB port.

Figure 3 shows the location of the battery compartment on the board.

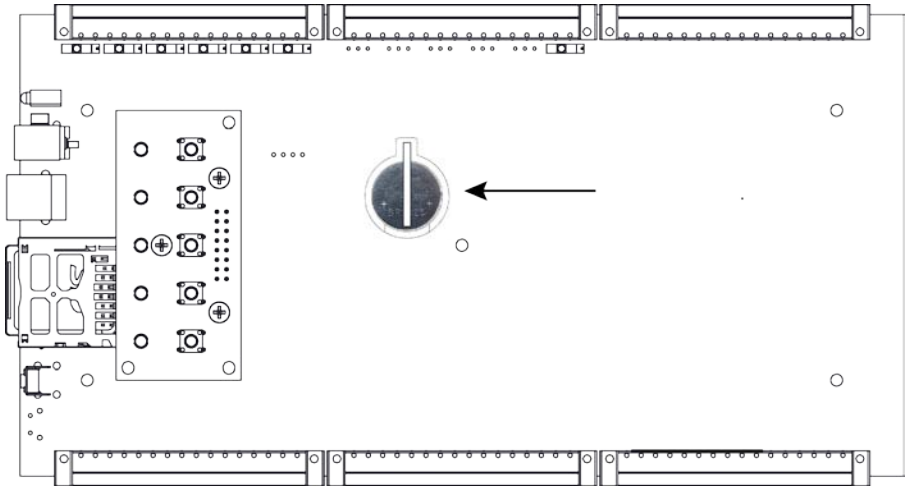


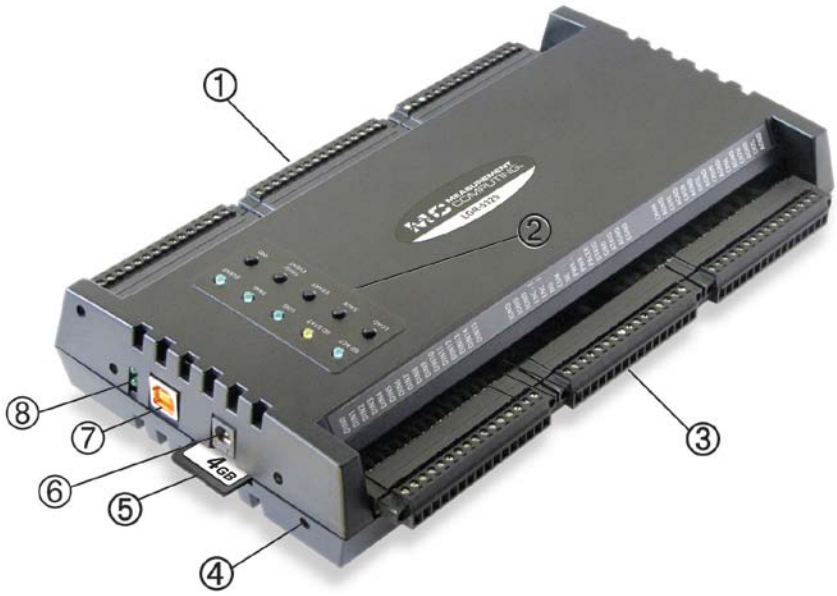
Figure 3. Location of battery compartment

5. Lift the clip and insert the new battery in the battery compartment. Make sure the positive side of the battery (+) is facing up and away from the circuit board.
6. Replace the top section of the case, and fasten it to the bottom section with the five screws.

Functional Details

External components

The external components of a LGR-5320 Series device shown in Figure 4 are explained in the following sections.



1	Screw terminals 1 through 48	5	SD card slot
2	Function buttons and LEDs	6	External power connector
3	Screw terminals 49 through 96	7	USB connector
4	Recessed reset button	8	Power LED (top) and USB activity LED (bottom)

Figure 4. LGR-5320 Series external components

Function buttons and LEDs (top of case)

Each function button on the top of a LGR-5320 Series device case is explained below. All buttons and LEDs are disabled when a LGR-5320 Series device is connected to a USB port.

- **SD ACT** LED—Blinks when data is read from or written to the SD card.

Caution! Do not remove the SD card when the **SD ACT** LED is blinking.

- **SD STAT** LED—Turns on for one second if you attempt an operation without inserting an SD card in the slot.

  The LED blinks when:

  - the logger detects an error on the SD card or SD drive
  - the configuration file on the SD card is invalid
  - a data overrun error has occurred when the device is logging data

When the **SD STAT** LED blinks to indicate an error, the four LEDs for analog channels CH0H, CHOL, CH1H, CH1L, and the four LEDs for analog channels CH6H, CH6L, CH7H, and CH7L blink in a pattern that represents a numeric error code. Press any button on the top of the case to acknowledge the error and stop the LEDs from flashing.

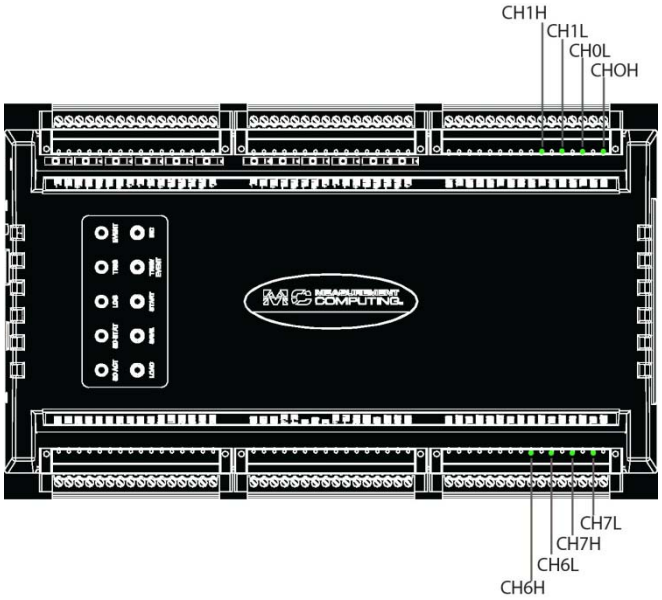


Figure 5. LGR-5320 Series error code LEDs

For example, if you attempt to log without an SD card inserted in a LGR-5320 Series device, the **CHOH** and **CH7L** LEDs both blink, representing binary code 0001.

All SD STAT errors and corresponding analog input LED blink codes are explained below.

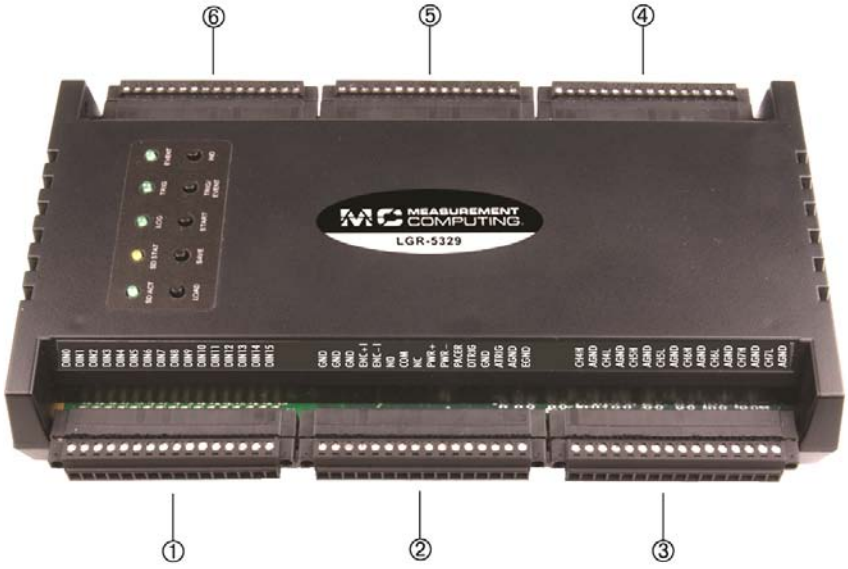
LGR-5320 Series error descriptions and codes

Error	**Blink code (binary)**	**LED pattern**			
		CH1L	**CH1H**	**CH0L**	**CH0H**
		CH6H	**CH6L**	**CH7H**	**CH7L**
Card not present	0001	○	○	○	●
Card not mounted	0010	○	○	●	○
Card write protected	0011	○	○	●	●
File system error	0100	○	●	○	○
FLASH write error	0101	○	●	○	●
Overrun – pacer	0110	○	●	●	○
Overrun – FIFO	0111	○	●	●	●
Overrun – events	1000	●	○	○	○
DMA error	1001	●	○	○	●
Card full	1010	●	○	●	○
File reached max size	1011	●	○	●	●
Log configuration error	1100	●	●	○	○
Log configuration not valid for device	1101	●	●	○	●

- **LOG** LED—On when the device is logging. Off when the device is idle.
- **TRIG** LED—Turns on when the acquisition is triggered.
- **EVENT** LED—Blinks when an event occurs.

- **IND** button—Cycles through and selectively enables/disables LEDs with each button press. By default, all LEDs are enabled when the device is powered on.
  - If you press the button when the LEDs are in their default setting, only the LEDs on top of the device are enabled.
  - If you press the button again, all LEDs are disabled.
  - If you press the button again, all LEDs are enabled.
- **TRIG/EVENT** button—Forces a trigger if logging has started and the device is waiting for a trigger. Adds an event to the event log if they are being recorded.
- **START** button—Starts logging when an SD card with a valid configuration file is in the SD card slot, and the device is disconnected from a USB port. When a device is logging data, pressing this button stops the data logging.
- **SAVE** button—Saves the current logging configuration to a file on the SD card.
- **LOAD** button—Loads the latest logging configuration file from the SD card.

Screw terminals and associated LEDs



1 Digital input terminals and LEDs
2 Digital trigger, pacer, isolated, earth, and analog ground terminals, and digital output state LED
3 Analog input 4–7, 12–15 (SE), 4–7 (Diff) terminals and LEDs
4 Analog input 0–3, 8–11 (SE), 0–3 (Diff) terminals and LEDs.
5 Counter input 0 and 1 terminals, LEDs, and configuration switches*
6 Counter input 2 and 3 terminals, LEDs, and configuration switches*

* Configuration switches only apply to quadrature counters and are only installed on the LGR-5327 and LGR-5329.

Figure 6. LGR-5320 Series screw terminals and LEDs

Figure 7. Screw terminal LED on

Screw terminal LED functions

The functions of the LEDs associated with screw terminals are explained below.

- The LED for each active digital connection is on when voltage is detected.
- The LED near the **PWR+** terminal is on when the relay is energized
- The LED for each analog input terminal is on if the associated channel is in the scan list.

On the LGR-5327 and LGR-5329, you can configure the encoder counter inputs as single-ended or differential mode using the switches that correspond to each pair of phase A, phase B, and Index terminals (see Figure 8).

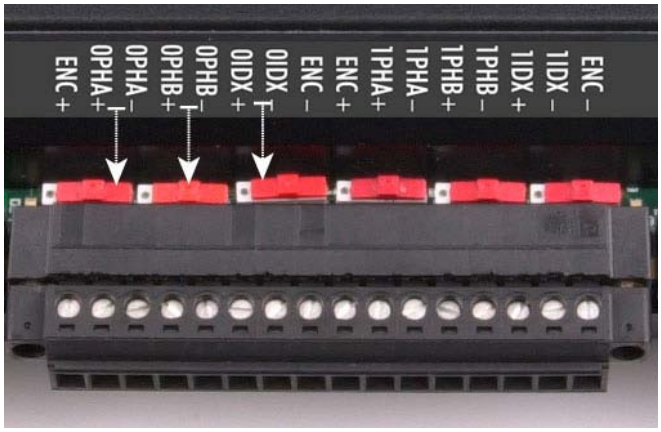


Figure 8. LGR-5327 and LGR-5329 counter channel input terminals and input mode switches

- To configure a counter channel for single-ended mode, slide the switch to the right. Note that the "dot" is visible on the switch when a channel is configured for single-ended mode.
- To configure a counter channel for differential mode, slide the switch to the left.

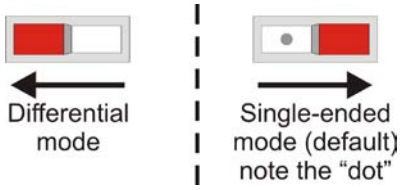


Figure 9. Channel input mode switch settings

Figure 9 assumes a board orientation with the USB connector on the right.

Signal connections

Analog input

LGR-5320 Series devices have a 16-bit, multiplexed A/D that supports up to 16 single-ended or up to eight differential analog inputs.

- For the LGR-5325, the maximum throughput sample rate is 100 kS/s.
- For the LGR-5327 and LGR-5329, the maximum throughput sample rate is 200 kS/s.

Analog input SE and DIFF channel configurations

Single-ended analog channels 0–3 **CH0H** = channel 0 SE **CH1H** = channel 1 SE **CH2H** = channel 2 SE **CH3H**= channel 3 SE	**Single-ended analog channels 8–11** **CH0L** = channel 8 SE **CH1L** = channel 9 SE **CH2L** = channel 10 SE **CH3L** = channel 11 SE
Single-ended analog channels 4–7 **CH4H** = channel 4 SE **CH5H** = channel 5 SE **CH6H** = channel 6 SE **CH7H**=channel 7 SE	**Single-ended analog channels 12–15** **CH4L** = channel 12 SE **CH5L** = channel 13 SE **CH6L** = channel 14 SE **CH7L** = channel 15 SE
Differential analog channels 0–3 **CH0H** /**CH0L** through **CH3H** /**CH3L**	**Differential analog channels 4–7** **CH4H** /**CH4L** through **CH7H** /**CH7L**

You can configure all LGR-5320 Series analog input channels for voltage input ranges of ±10 V, ±5 V, or ±1 V.

The LGR-5327 and LGR-5329 also support a ±30 V voltage input range.

Unused analog input channels can either be left floating or connected to an **AGND** pin.

When using the ±30 V input range with the LGR-5327 and LGR-5329, keep source impedance and source capacitance as small as possible to minimize settling time, gain, and bandwidth errors.

When connecting differential inputs to floating voltage sources in the ±10 V, ±5 V, ±1 V ranges, the user must provide a DC return path from the *low channel* (CH*x*L) connector of each differential input to ground. To do this, simply connect a resistor from the CH*x*L connector of the differential inputs to AGND. A value of approximately 100 kΩ can be used for most applications.

- On the LGR-5325, the **AGND** and **GND** terminals are tied together internally. These grounds are electrically isolated from the **EGND** (earth ground) terminal block pin.
- On the LGR-5327, the **AGND, ENC,** and **GND** terminals are tied together internally. These grounds are electrically isolated from the **EGND** terminal block pin.
- On the LGR-5329, the **AGND, ENC,** and **GND** terminals are tied together internally. These grounds are electrically isolated from the **EGND** and the **IGND** (isolated ground) terminal block pins.

Trigger input

The LGR-5320 Series supports the following trigger modes to accommodate certain measurement situations.

- External digital trigger
- External analog trigger (single-channel)
- Digital pattern trigger

The LGR-5327 and LGR-5329 also support multichannel analog trigger mode.

To manually trigger an acquisition, press the **TRIG/EVENT** button.

Digital and analog triggers connected

The input of the digital trigger and the output of the single-channel analog signal comparator are connected directly to hardware circuits to provide low-latency triggering. Latencies should be low (around 1.5 µs).

External digital trigger

A digital (or TTL-level) trigger starts an acquisition when the trigger condition is met at the **DTRIG** terminal.

When using digital triggering, the TTL trigger signal on the **DTRIG** connector is for a trigger condition. When the selected condition occurs, it is the trigger event.

If the LGR-5320 Series device is ready for a trigger, then the trigger event occurs.

If the LGR-5320 Series device is not ready due to one of the following reasons, the trigger is ignored:

- Incomplete configuration
- The device is finishing the previously triggered acquisition

LGR-5320 Series devices do not indicate when a trigger is ignored.

External analog trigger (single-channel)

The input signal on the **ATRIG** terminal is compared to a programmable analog trigger level.

- If the analog input trigger condition is met, the LGR-5320 Series device generates an internal trigger signal.
- If the device is ready for a trigger, then the trigger event occurs.
- If the device is not ready—due to incomplete configuration, or because the device is finishing the previously triggered acquisition—the trigger is ignored.

LGR-5320 Series devices do not indicate when a trigger is ignored.

Hysteresis—The analog trigger circuit has hysteresis to reduce the occurrence of false triggering due to input noise.

Hysteresis is the range that a signal must pass through before a trigger is generated. This prevents false triggers from happening when small amounts of noise exist on the signal.

Figure 10 shows the hysteresis effect for a rising-edge trigger.

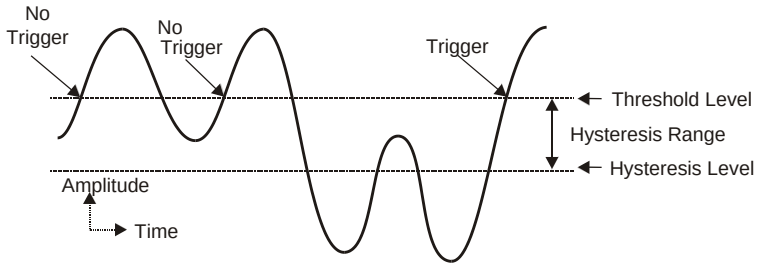


Figure 10. Hysteresis effect on a rising-edge trigger

A trigger occurs when the analog input rises above the trigger level, or *threshold* –but only after the input level has been below the hysteresis range. If the level briefly drops just below the threshold—perhaps due to noise – and then rises above it again, no trigger occurs, since the signal did not drop below the hysteresis range.

After the level drops below hysteresis, it can then produce a trigger by rising above the threshold.

Multichannel trigger (LGR-5327 and LGR-5329 only)

A multichannel trigger event is a combination of measured channel values.

The FPGA samples the specified channels, and if programmable conditions are met, triggers the acquisition. Multichannel triggering examines digitized data, and the trigger latencies are much greater than the external analog and digital triggers.

If minimum trigger latency is not critical in your application, you may be able to take advantage of multichannel triggering.

The FPGA looks at (scans) digitized input channels and examines each one to determine if it meets programmed levels for a valid trigger. This multichannel triggering is a two-step process:

1. The FPGA examines each of its specified input signals to determine if the trigger is valid.
2. After all of the channels have been examined, the FPGA logically combines the individual triggers to generate the actual trigger. You can program the FPGA to generate a trigger if any individual trigger is valid (OR) or if all triggers are valid (AND) (see Figure 11)

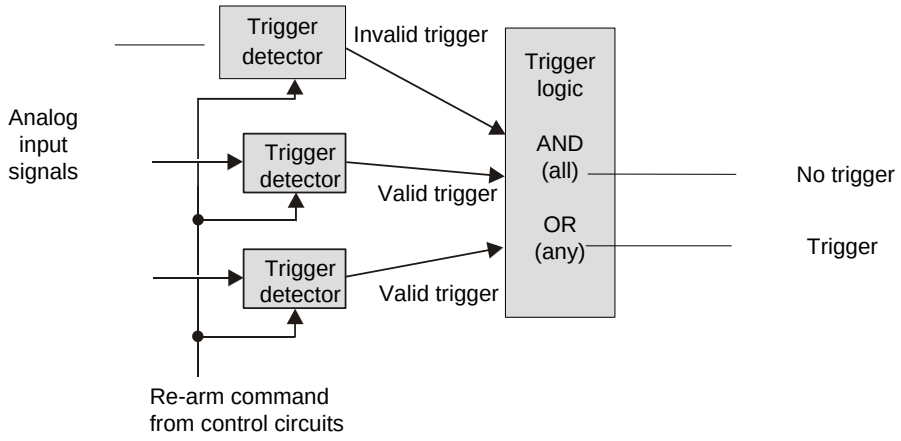


Figure 11. Multichannel trigger detection

The logical relationship among three elements—polarity, duration, and initialization—determine if a trigger is valid in a multichannel environment.

Analog trigger types (LGR-5325) and multichannel trigger types (LGR-5327/5329)

Each trigger type is a combination of three elements: *slope*, *duration*, and *initialization*.

Slope (above/rising or below/falling)—Sets whether the trigger is valid when the signal is *above the threshold* (rising) or *below the threshold* (falling).

Duration (instantaneous or latched)—Specifies the action to take if the signal level becomes invalid after it has been valid:

- *Instantaneous triggers* are valid in scans where that channel trigger condition is met. They can become invalid in subsequent scans when the trigger condition is not met.

  With the LGR-5327 and LGR-5329, instantaneous triggers are used to trigger when all channels triggers are valid (multichannel "AND" mode) or when any of the channel trigger conditions are valid (multichannel "OR" mode).
- *Latched triggers* remain valid until the acquisition is complete. These trigger types are used to trigger scans when two or more signals have already become valid.

  With the LGR-5327 and LGR-5329, you can use a combination of instantaneous and latched triggers in multichannel triggering.

  The trigger duration only makes a difference in multichannel *AND* triggering.

  In multichannel "OR" triggering, the acquisition is triggered as soon as any channel becomes valid—what happens when a channel becomes invalid does not matter.

  In contrast, "AND" triggering waits for all triggers to be valid, making latching important for rapidly changing signals.

Initialization (level or edge)—Specifies the sequence necessary for a signal to be a valid trigger:

- *Level triggers* become valid when they reach or exceed the threshold, even if they are already past the threshold when the acquisition starts.
- *Edge triggers* first wait until the signal level is invalid. Then they wait for the signal to reach the threshold before becoming valid. Thus, level triggers look for a signal level, whenever it occurs, and edge triggers look for a rising or falling transition that reaches the threshold.

The first step in both multichannel and analog triggering is to examine the input signals. To determine trigger validity, the FPGA can examine each input signal in one of eight ways. Refer to the following table.

LGR-5325, LGR-5327, LGR-5329 trigger signal attributes

Trigger type	Slope	Duration	Initialization
Above-level	N/A	Instantaneous	Level
Below-level	N/A	Instantaneous	Level
Above-level-with-latch	N/A	Latched	Level
Below-level-with-latch	N/A	Latched	Level
Rising-edge	Rising	Instantaneous	Edge
Falling-edge	Falling	Instantaneous	Edge
Rising-edge-with-latch	Rising	Latched	Edge
Falling-edge-with-latch	Falling	Latched	Edge

The input signals are compared a specified signal level.

Above-level trigger—This trigger is valid whenever the signal goes above the specified level, and stays valid until the signal goes below the level.

In Figure 12, the channel trigger is valid during the two shaded intervals.

With the LGR-5327 and LGR-5329, whether or not this condition triggers an acquisition depends on the type of multichannel triggering (*AND* or *OR*) and on the state of other trigger channels.

- With *OR* multichannel triggering, the LGR-5327 and LGR-5329 triggers a scan when the signal first rises above the threshold. If the device is ready and the condition is met, the scan is triggered.
- With *AND* multichannel triggering, the LGR-5327 and LGR-5329 does not trigger a scan until every specified trigger channel is valid. If all other trigger channels are valid, the device triggers an acquisition when the signal reaches the shaded region. If some channels are not valid, however, this channel has no effect.

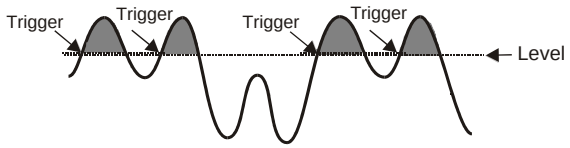


Figure 12. Above level initialization, instantaneous duration

Below-level trigger—This trigger is valid whenever the signal level is below the level and stays valid until the signal goes above the level—the opposite of above-level triggering.

With the LGR-5327 and LGR-5329, as with all multichannel trigger types, the acquisition's actual trigger depends on the combination of this trigger with the other channels' trigger states.

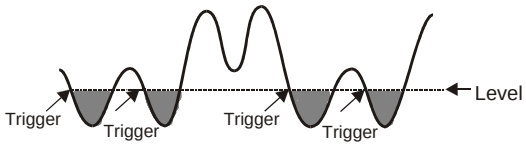


Figure 13. . Below level initialization, instantaneous duration

Above-level-with-latch trigger—With this trigger type, the channel becomes valid when the signal level is above the threshold, and remains valid until the acquisition is complete and re-armed.

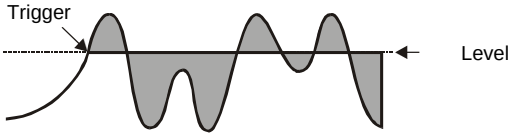


Figure 14. Above level initialization, latched duration

Below-level-with-latch trigger—With this trigger type, the channel becomes valid when the signal level is below the threshold and remains valid until the acquisition is complete and re-armed—the opposite of above-level-with-latch triggering). Latched triggers are often used in multichannel "AND" triggering—the acquisition does not trigger until all trigger channels are valid. After a latched trigger becomes valid, it stays valid and waits for the other triggers to become valid until the acquisition is triggered and completed.

If the trigger is not latched, the channel may not stay valid. A LGR-5320 Series device does not trigger the acquisition until the channel becomes valid again, and all channels simultaneously reach their thresholds.

Latched triggering is used to trigger an acquisition after an event has occurred, while non-latched triggering is used only during the simultaneous occurrence of desired signal levels. It is possible to combine different trigger types in a single multichannel trigger.

For example, by configuring channel 3 for below-level triggering, and channel 2 for above-level-with-latch triggering, the device could trigger the acquisition when channel 3 is below 0.9 V after channel 2 has gone above –1.3 V.

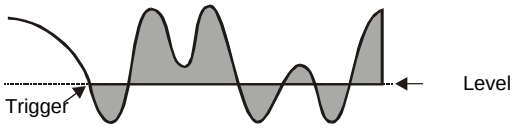


Figure 15. Below level initialization, latched duration

Rising-edge trigger—This trigger becomes valid after the signal level has been below the hysteresis range and then goes above the threshold. This trigger becomes invalid when the signal level goes below the hysteresis range. Unlike above-level triggering, the channel cannot become valid until the signal level first goes below the hysteresis range. This prevents the false triggering that would occur if the signal were above the threshold at the start of the acquisition.

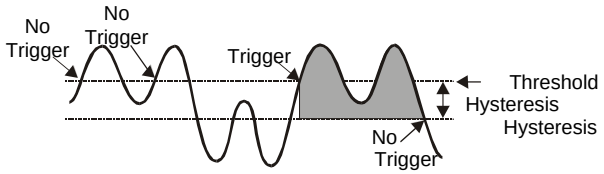


Figure 16: Rising edge, instantaneous duration, edge initialization

Falling-edge trigger—This trigger is the reverse of the rising-edge trigger: the trigger becomes valid after the signal level has been above the hysteresis range and then goes below the threshold. This trigger becomes invalid whenever the signal level goes above the hysteresis range. This prevents the false triggering that would occur with below-level triggering if the signal was below the threshold at the start of the acquisition.

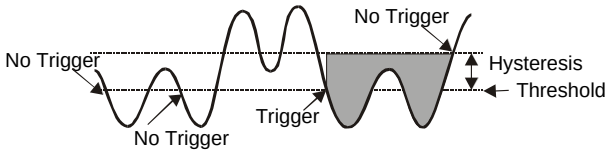


Figure 17: Falling slope, instantaneous duration, edge initialization

Rising-edge-with-latch trigger—This trigger becomes valid like a rising-edge trigger—when the signal level goes above the threshold after first being below the hysteresis range. However, the rising-edge-*with-latch* trigger does not become invalid, regardless of the signal level, until the acquisition is complete. Rising-edge-with-latch is used to trigger after the channel has reached the threshold, rather than just while the channel is above the threshold.

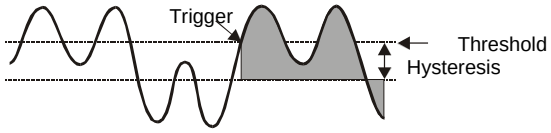


Figure 18: Rising slope, latched duration, edge initialization

Falling-edge-with-latch trigger—This trigger is the reverse of the rising-edge-with-latch trigger—it becomes valid after the signal level has been above the hysteresis range and then goes below the threshold. The trigger remains valid until the acquisition is complete.

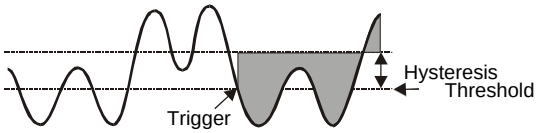


Figure 19: Falling slope, latched duration, edge initialization

Digital pattern trigger

The digital pattern trigger is an expanded digital-trigger that starts collecting data when a 1 to 16-bit digital pattern—that you define with *pattern* and *mask* settings—matches the bit pattern on the digital input connector.

This type of trigger is useful when trying to capture noise, vibrations, or some other physical disturbance that occurs at a particular point in a digitally-sequenced process, such as a relay-logic-control system.

Two settings control this trigger operation—the *condition* and the *mask*.

- The *polarity* setting allows the following choices:

  Rising edge/high level (equal to)—Triggers when there is an exact pattern matches of "1s" and "0s" between the compared patterns.

  Falling edge/low level (not equal to)—Triggers on any change of "1s" and "0s" between two patterns that previously matched.
- The *mask* setting can set any of the input bits to *don't care* (X), which excludes that bit from the polarity comparison.

Digital I/O

You can connect up to 16 digital inputs to a LGR-5320 Series device. Each digital input is electrically isolated from the host computer and from the LGR-5320 Series analog and counter circuits.

You can configure these inputs to detect events based on change of state or pattern recognition. These are the same bits used for a digital pattern trigger (refer to the *Digital-pattern trigger* section above)

The digital inputs have a wide input voltage range of 0 V to 30 V.

The digital output is an alarm implemented as a single Form C relay on the **NC** (normally closed), **COM** (common), and **NO** (normal open) screw terminals.

You can configure the relay to energize when the trigger condition is met and data is being recorded.

Always use the IGND screw terminals with digital inputs with the LGR-5329

Because the digital inputs on a LGR-5329 are electrically isolated from the analog and digital I/O circuitry, always use the IGND (isolated ground) screw terminals as the ground return for digital inputs.

Counter input

LGR-5320 Series devices can read counter inputs as part of a digital scan group.

When read as part of a scan, the count of each channel counter is set to 0 and latched at the beginning of the acquisition. Each clock pulse (*start-of-scan* signal) initiates a scan of all channels specified. Each time a LGR-5320 Series devices receives a *start-of-scan* signal, the counter values are latched and are available to the device. The values returned during scan period 1 are always zero. The values returned during scan period 2 reflect what happened during scan period 1. The scan period defines the timing resolution. To achieve a higher timing resolution, shorten the scan period.

LGR-5320 Series devices support the following counter input modes:

- Counter (general event counting)
- Period counting
- Pulse width counting
- Edge-to-edge timing
- 1X, 2X, and 4X encoder counting.
- Up/down counting

Counter operation modes are programmable with software. Some modes use the user-configurable **ModuloN** mode. This number does not directly affect the current count, but sets a limit used in some modes to determine counter behavior.

All counter modes use the Phase A input. Some modes also make use of the Phase B and Index inputs. The counter signal names on the LGR-5325 are CTRx, UPDNx and GATEx.

Each mode supports additional sub-modes for counter operations. Refer to the discussion of each counter mode in the pages that follow for specific information.

Encoder mode (LGR-5327 and LGR-5329 only)

The LGR-5327 and LGR-5329 can simultaneously decode signals from up to four encoders with 16 or 32-bit counters and X1, X2, and X4 count modes.

Both of these devices provide Phase A (±), Phase B (±), and Index (±) inputs for each connected encoder (0°, 90°, and zero). Phase A and Phase B are generated at a 90° phase shift with respect to each other.

The LGR-5327 and LGR-5329 use Phase A and Phase B signals to determine:

- system position (counts)
- velocity (counts per second)
- direction of rotation (B leading or lagging A)

You can program the Index signal to gate, latch the current count, or clear/reload the counter with the *modulo* number.

You can use the Index signal to establish an absolute reference position within one count of the encoder rotation (360°).

Each input can be debounced from 500 ns to 25.5 ms (total of 16 selections) to eliminate extraneous noise, or switch induced transients. Encoder input signals must be within ±12 V, and the switching threshold is 200 mV differential, or 200 mV above 3.0 V and 50 mV_{typ} hysteresis. Refer to Debounce mode on page 24 for additional information.

The following options provide different levels of accuracy with respect to the encoder position:

Encoder mode options

Encoder mode	Description
1X	Counts rising edges on phase A. In 1X mode the encoder position is accurate to within 360° ÷ *encoder count* (for example, if using a 512-count encoder, accuracy would be 360° ÷ 512)
2X	Counts rising edges and falling edges on phase A. In 2X mode the encoder position has double accuracy (360° ÷ (*encoder count* * 2)).
4X	Count rising and falling edges on both phase A and phase B. In 4X mode the encoder position has quadruple accuracy (360° ÷ (*encoder count* * 4)).

Modulo mode options (Encoder mode)

Modulo mode	Description
Rollover	Counting up: When the maximum count (specified by the *modulo* number) is reached, the counter rolls over to 0 and continues counting up. Counting down: When the count reaches 0, the counter rolls over to the maximum count (specified by the *modulo* number) and continues counting down.
Range limit	When counting up: The counter stops when the maximum count (specified by the *modulo* number) is reached. Counting resumes if direction reverses or counter is cleared. When counting down: The counter will count down to 0 and then stop. Counting resumes if direction reverses or the counter is cleared.
Non-recycle	The counter is disabled if a count overflow or underflow occurs or the *modulo* number is reached. A clear command (via software or Index input) is required to re-enable the counter.

Some Encoder mode options are specific to the Index signal. These modes are explained below.

Index input mode options (Encoder mode)

Index mode	Description
No-Op	Ignore the counter index.
Clear	Reloads the count with the modulo number when the counter clears on the rising or falling edge (software selectable) of the Index signal.
Gate	Use the Index signal to gate the counter.
Latching	Use the Index signal to latch the counter.

Counter mode

You can use a LGR-5320 Series device as a high-speed pulse counter for general counting applications.

Each counter is a 32-bit counter, and accepts frequency inputs up to 10 MHz.

In counter mode, phase A is the primary counter input. You can use phase B to set the count direction in up/down counting. Use the Index input to gate, latch, or decrement the counter.

LGR-5320 Series devices read counter inputs synchronously as part of the scan list, and support the following options in counter mode:

Counter mode options

Counter mode	Description
Totalize	General pulse counter.
Clear on read	The counter clears after each synchronous read. The counter value is latched and returned before it clears.

Modulo mode options (Counter mode)

Counter mode	Description
Range limit	When counting up: The counter stops when the maximum count—specified by the *modulo* number—is reached. Counting resumes if the direction reverses or the counter reloads. When counting down: The counter counts down to 0 and then stops. Counting resumes if the direction reverses or the counter reloads.
Non-recycle	The counter is disabled if a count overflow or underflow occurs, or the *modulo* number is reached. A clear command issued through software or through the Index input is required to re-enable the counter.
Up/down	Up/down counting mode uses phase A as the pulse source and phase B as the direction. The counter counts up when phase B=1 (high), and counts down when phase B=0 (low).
Modulo-N	Sets the specified *modulo* number used by the counter mode options explained in this table.

Some counter mode options are specific to the Index signal. These modes are explained in the following table.

Index input mode options (counter mode)

Index mode	Description
Gating	Gating mode allows the Index input to gate the counter. The counter is enabled when the Index signal is high. When the Index signal is low, the counter is disabled, but holds the count value.
Latching	Latching mode allows the Index signal to latch the count.
Decrement	Decrement mode allows the Index signal to decrement the counter.

Period measurement mode

Use period mode to measure the period of a signal at a counter channel phase A input. You can measure 1X, 10X, 100X or 1000X periods, 16-bit or 32-bit values. Four resolutions are available—to 20 ns, 200 ns, 2 µs, or 20 µs. All period measurement mode options are software-selectable. LGR-5320 Series devices use the 50 MHz system clock as the timing source, and measure periods from sub-microsecond to many seconds.

LGR-5320 Series devices read counter channel inputs synchronously using period mode.

Pulse width measurement mode

Use pulse width mode to measure the time from the rising edge to the falling edge--or vice versa--on a signal on a phase A counter input. Four resolutions are available (20 ns, 200 ns, 2 µs, or 20 µs). All pulse width measurement mode options are software selectable. LGR-5320 Series devices use the 50 MHz system clock as the timing source. Pulse widths from sub-microsecond to many seconds can be measured.

LGR-5320 Series devices use read counter channel inputs synchronously using pulse width mode.

Timing measurement mode

Measures the time from a rising or falling edge on phase A to a rising or falling edge on the Index inputs.

Debounce mode

LGR-5320 Series devices have debounce circuitry, which eliminates switch-induced transients that are typically associated with electromechanical devices including relays, proximity switches, and encoders.

All debounce options are software selectable. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity. LGR-5320 Series devices use can debounce each channel with 16 programmable debounce times in the range of 500 ns to 25.5 ms.

Two debounce modes (*trigger after stable* and *trigger before stable*) and a debounce bypass are shown in Figure 20. The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is makes the input rising-edge or falling-edge sensitive.

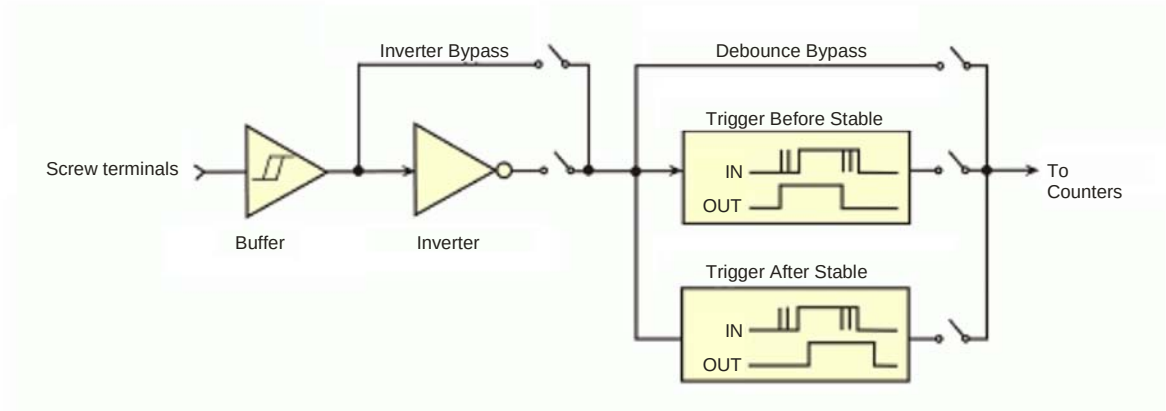


Figure 20. Debounce block diagram

Edge selection is available with or without debounce. In this case, the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

Trigger after stable mode—In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time. Refer to Figure 21.

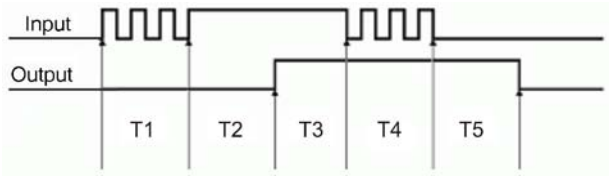


Figure 21. *Trigger after stable* mode

T1 through T5 indicate time periods. In *trigger after stable* mode, in order for that edge to be accepted (passed through to the counter module), the input signal to the debounce module is required to have a period of stability after an incoming edge. For this example, the debounce time is equal to T2 and T5.

- T1—In Figure 21, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2—At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time—therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output, and the entire disturbance on the input would have been rejected.
- T3—During time period T3, the input signal remained steady. No change in output is seen.
- T4—During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5—At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time—therefore the output goes low.

Trigger before stable mode—In the *trigger before stable* mode, the output of the debounce module immediately changes state, but does not change again until a period of stability has passed. For this reason, you can use this mode to detect glitches. Refer to Figure 22.

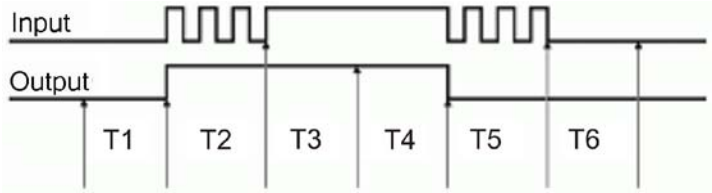


Figure 22. *Trigger before stable* mode

T1 through T5 in Figure 22 indicate time periods:

- T1—The input signal is low for the debounce time (equal to T1); therefore, when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.
- T2—During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3—During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4—At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5—During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6—After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce mode comparisons—Figure 23 shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Use the **bypass** option to achieve maximum glitch recognition.

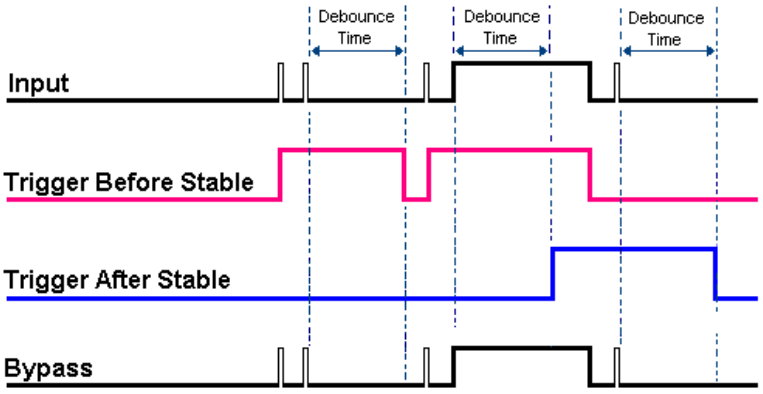


Figure 23. Example of two debounce modes interpreting the same signal

Set the debounce time according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time that is too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, view the analog waveform along with the counter output. You can do this by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The *trigger before stable* mode recognizes and counts the first glitch within a group, but rejects the

subsequent glitches within the group if the debounce time is set accordingly. Set the debounce time to encompass one entire group of glitches, as shown in Figure 24.

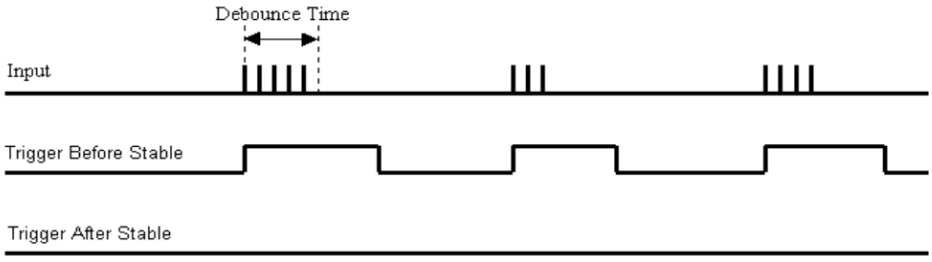


Figure 24. Optimal debounce time for *trigger before stable* mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. Use *Trigger after stable* with electromechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse, but longer than the period of the undesired disturbance, as shown in Figure 25.

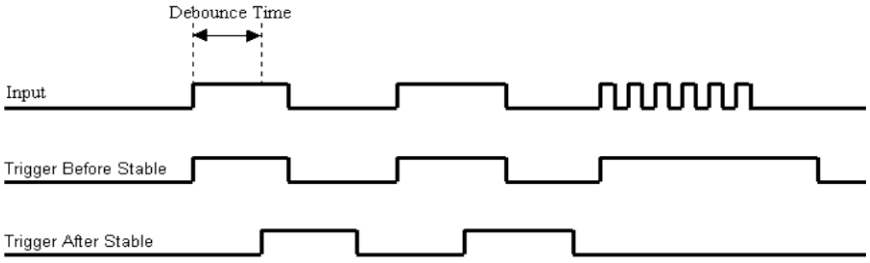


Figure 25. Optimal debounce time for *trigger after stable* mode

Mechanical drawings

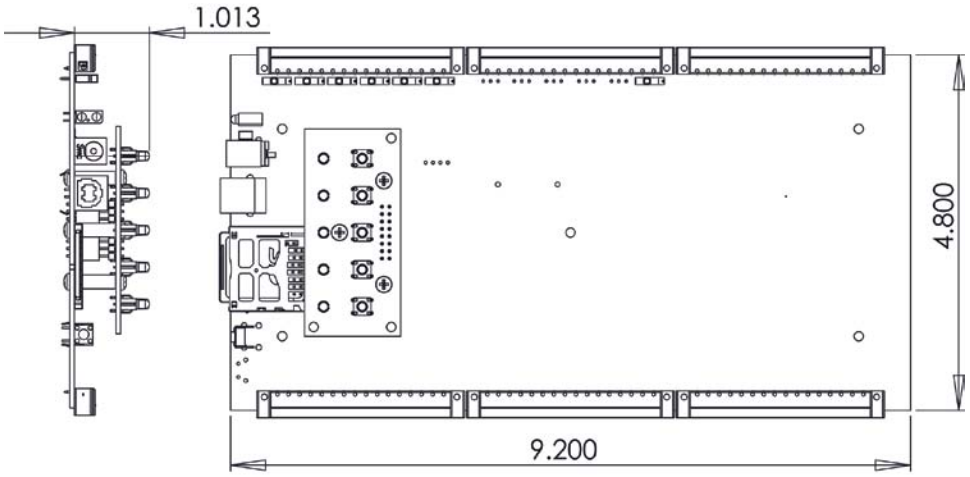


Figure 26. Circuit board dimensions

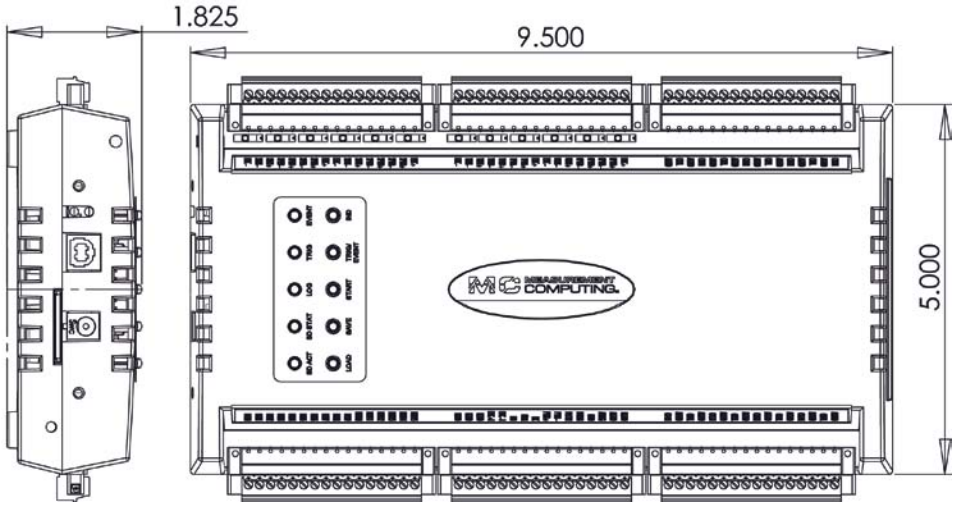


Figure 27. Housing dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Condition	Specification
A/D converter		16-bit successive approximation type
Input ranges	Software selectable per channel	LGR-5327/5329: ±30 V, ±10 V, ±5 V, ±1 V LGR-5325: ±10 V, ±5 V, ±1 V
Number of channels		8 differential (DIFF)/16 single-ended (SE), software-selectable
Input configuration		Multiplexed
Absolute maximum input voltage	*CHx_x to AGND*	LGR-5327/5329: ±*38 V max(power on and power off)* LGR-5325: ±*25 V max(power on and power off)*
Input impedance	±*30 V range* (LGR-5327/5329 only)	*1 MΩ (power on),* *1 GΩ (power off)*
	±*10 V, ±5 V, ±1 V range*	*10 GΩ (power on)* *1 GΩ (power off)*
Input leakage current		±*100 pA*
Input capacitance	±30 V range (LGR-5327/5329)	*90 pf (Note 2)*
	±10 V, ±5 V, ±1 V range	*55 pf*
Maximum working voltage (signal+ common mode)	±30 V range	±30.05 V
	±10 V, ±5 V, ±1 V range	±10.2 V
Common mode rejection ratio	fin = 60 Hz, ±30 V range	65 dB min
	fin = 60 Hz, all other ranges	75 dB min
Crosstalk	DC to 25 kHz, adjacent DIFF mode channels	–80 dB
ADC resolution		16 bits
Input bandwidth (–3 dB)	All input ranges	450 kHz min
Input coupling		DC
Maximum sample rate		LGR-5327/5329: 200 kS/s LGR-5325: 100 kS/s
A/D pacing sources		See Input sequencer section
Warm up time		30 minutes, min
Absolute accuracy	All ranges	0.07% FSR
Noise	DIFF mode	2 LSB rms

Note 1: Unused analog input channels can either be left floating or tied to an AGND pin.

Note 2: When using the ±30 V input range, keep source impedance and source capacitance as small as possible to minimize settling time, gain, and bandwidth errors.

Note 3: When connecting differential inputs to floating voltage sources in the ±10 V, ±5 V, ±1 V ranges, the user must provide a DC return path from the *low channel* (CH*x*L) connector of each differential input to ground. To do this, simply connect a resistor from the CH*x*L connector of the differential inputs to AGND. A value of approximately 100 kΩ can be used for most applications.

The ±30 V input range on the LGR-5327/5329 incorporates an input resistor attenuator network, which eliminates the need for external bias return compensation resistors.

Note 4: The LGR-5325 AGND and GND pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.
The LGR-5327 AGND, GND and ENC- pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.
The LGR-5329 AGND, GND and ENC– pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) and the IGND (isolated ground) pins.

Analog input calibration

Table 2. Analog input calibration specifications

Parameter	Specifications
Calibration method	Factory calibration
Calibration interval	1 year

External clock input

Table 3. External clock I/O specifications

Parameter	Condition	Specification
External clock I/O		PACER (pin 75), software-selectable as input or output
Input high voltage		2.2 V max
Input low voltage		0.6 V min
Output high voltage	IOH = –8 mA	3.8 V min
Output low voltage	IOL = 8 mA	0.4 V max
Pacer rate		LGR-5325: 100 kHz max LGR-5327/5329:200 kHz max
Minimum pulse width		2.5 us min

Input sequencer

Table 4. Input sequencer specifications

Parameter	Specifications
Pacer clock sources: two	■ Internal LGR-5325: 10 µs to 85.9 sec in 20 ns steps LGR-5327/5329: 5 µs to 85.9 sec in 20 ns steps ■ External (PACER) LGR-5325: 10 µs min LGR-5327/5329: 5 µs min
Programmable parameters per scan	■ Channel type (DIFF analog, single ended analog, counter, digital input) ■ Channel number (random order) ■ Gain Any channel specified with a ±30 V range (LGR-5327/5329 only) cannot be specified with any other range in the sequence
Depth	512 locations
Pacer interval	LGR-5325: 10 µs min (100 kHz max pacer rate) LGR-5327/5329: 5 µs min (200 kHz max pacer rate)
Channel to channel sampling period (scan clock)	LGR-5325: 10 µs, fixed (analog inputs) LGR-5327/5329: 5 µs , fixed (analog inputs) All specified digital channels (counters, digital inputs) are sampled simultaneously at the beginning of the pacer interval

Triggering

Table 5. Triggering specifications

Parameter	Condition	Specification
Mode	External digital through DTRIG (pin 76)	Software configurable for rising or falling edge.
	External analog through ATRIG (pin 78)	See Table 6
	Multi-channel analog (LGR-5327/5329 only)	Level-sensitive based on acquired data. Up to 16 channels may be used as independent trigger sources.
	Digital pattern trigger (LGR-5327/5329 only)	Trigger when a user-defined 1 to 16 bit digital pattern is matched on the DIN0–DIN15 pins. Programmable mask bits.
External digital trigger latency	Non-pretrigger acquisition	100 ns typ, 1 µs max
	Pretrigger acquisition	1 scan period max
External trigger pulse width		1 µs min
Internal trigger latency		2 * (1/per-channel sample rate)

External analog trigger

Table 6. External trigger specifications

Parameter	Conditions	Specification
External analog trigger source		ATRIG input (pin 78)
Analog trigger input ranges		LGR-5325: ±10 V LGR-5327/5329: ±30 V, ±10 V, software-selectable
Absolute maximum input voltage	*ATRIG_IN to AGND*	LGR-5325: *±25 V V max (power on and power off)* LGR-5327/5329: *±38 V max (power on and power off)*
Input impedance	*±30 V range* (LGR-5327/5329 only)	*1 MΩ (power on/off)*
	±10 V range	*10 GΩ (power on)* *1 GΩ (power off)*
Trigger modes		Configurable for: ■ Positive or negative slope ■ Level
Trigger/hysteresis resolution		12 bits, 1 in 4096
Trigger/hysteresis levels		LGR-5325: ±10 V/4096 LGR-5327/5329: ±10 V/4096 or ±30 V/4096, software selectable
Trigger/hysteresis accuracy		±2% of reading, ±50 mV offset
Latency		1.5 µS
Full power bandwidth (–3 dB)		1 MHz

Digital input

Table 7. Digital Input specifications

Parameter	Specification
Number of inputs	16 channels
Input voltage range	■ LGR-5325/5327: 0 V to 28 V ■ LGR-5329: 0 V to 30 V
Input type	■ LGR-5325/5327: TTL ■ LGR-5329: Industrial
Input characteristics	■ LGR-5325/5327: 47 kΩ pull-down resistor, 39.2 kΩ series resistor ■ LGR-5329: Resistor divider 39.2 kΩ series resistor and 10 kΩ shunt resistor connected to IGND
Isolation (LGR-5329 only)	500 VDC min (Note 6)
Maximum input voltage level	■ LGR-5325/5327: 32 V (power on/off) ■ LGR-5329: 36 V (power on/off)
Minimum high-level input voltage threshold	■ LGR-5325/5327: 2.0 V max ■ LGR-5329: 10.04 V max
Maximum low-level input voltage threshold	■ LGR-5325/5327: 0.8 V min ■ LGR-5329: 3.85 V min
Event logging (LGR-5327/5329 only)	Change of state, pattern recognition. Event time stamped using real time clock.

Note 5: The digital inputs are electrically isolated from the analog and digital I/O circuitry. The IGND (isolated ground) pins should be used as the ground return for the digital inputs.

Digital output

Table 8. Digital output specifications

Parameter	Specification
Number of outputs	1
Type	Mechanical relay, NEC ED2/EF2 series
Relay configuration	1 Form C
Relay contact resistance	0.075 Ω
Relay contact operate time	3 ms (excluding bounce)
Relay contact release time	2 ms (excluding bounce)
Relay insulation resistance	1000 MΩ at 500 VDC
Relay contact ratings	Maximum switching voltage: 220 VDC/250 VAC
	Maximum switching current: 1.0 A
	Maximum carrying current: 2.0 A

Fault tolerance

Table 9. Fault condition behavior

Condition	Behavior
Power loss	■ Volatile memory data loss (internal memory) ■ Data loss if data being written to non-volatile storage. MCC cannot guarantee integrity of existing data on storage device. (Note 6)
Unexpected removal of SD card	■ Data loss if data being written to non-volatile storage. MCC cannot guarantee integrity of existing data on storage device. (Note 6)
Power on after fault.	■ Unit restarts with existing configuration.

Note 6: Solid-state memory devices behave differently under fault conditions. MCC cannot guarantee the integrity of data, both new and existing, in the event of power loss, unexpected media removal or similar actions.

Counters

Table 10. Counter specifications

Parameter		Condition	Specification
Counter type			■ LGR-5325: Conventional ■ LGR-5327/5329: Conventional and Quadrature (x1, x2, x4)
Number of channels			4
Inputs			LGR-5325: Counter, Up/Down, Gate LGR-5327/5329: Phase A+/A–, Phase B+/B–, Index +/–
Resolution (programmable)			32-bit or 16-bit.
Count Modes			Up/down counting
			Period/frequency counting
			Modulo-N
			Quadrature counting (LGR-5327/5329 only)
Debounce times (programmable)			16 steps from 500 ns to 25 ms; positive or negative edge sensitive; glitch detect mode or debounce mode
Timebase accuracy			50 ppm
LGR-5325 only	Input voltage range		0 V to 5.5 V
	Input type		TTL
	Input characteristics		49.9 KΩ pull-down resistor
	Maximum input voltage range		–0.5 V to 7.0 V
	Input high voltage		2.0 V
	Input low voltage		0.8 V
LGR-5327/ 5329 only	Receiver type		Quad DIFF receiver
	Configuration		Each channel consists of Phase A input, Phase B input and Index input, with each input switch selectable as SE or DIFF.
		DIFF	■ Phase A, Phase B and Index (+) inputs at user connector routed to (+) inputs of the DIFF receiver. ■ Phase A, Phase B and Index (–) inputs at user connector routed to (–) inputs of the DIFF receiver.
		SE	■ Phase A, Phase B and Index (+) inputs at user connector routed to (+) inputs of DIFF receiver. ■ Phase A, Phase B and Index (–) inputs at user connector routed to ground. ■ (–) inputs of DIFF receiver routed to +3 V reference.
	Common mode input voltage range		±12 V max
	Differential input voltage range		±12 V max
	Input sensitivity		±200 mV
	Input hysteresis		50 mV typ
	Input impedance		12 kΩ min
	Absolute maximum input voltage	DIFF	±14 V max

Device configuration

Table 11. Configuration

Parameter	Specification
Local	Host PC over USB
Remote	Through configuration file on SD card
Configuration file format	Binary

Controls/indicators

Table 12. Controls/indicators

Parameter	Specification
LOAD button	Loads a configuration from the SD card/enters USB bootloader (hold while applying power)
SAVE button	Saves configuration to the SD card
START button	Starts an acquisition
TRIG/EVENT button	Forces a trigger / logs an event
IND button	Turns LED indicators on/off in 3 steps: All on – Top indicators only – All off
Reset button	Resets the device
SD ACT indicator	Indicates SD card read/write activity
SD STAT indicator	Indicates SD card/device error condition if blinking
LOG indicator	Indicates acquisition in progress
TRIG indicator	Indicates trigger occurred
EVENT indicator	Flashes when an event is logged or configuration is loaded or saved
Power indicator	(Top LED on case end) Indicates power is good and device is ready
USB indicator	(Bottom LED on case end) Indicates USB connection is active, blinks off for USB activity
Analog input indicators	Indicates corresponding analog input is in the acquisition
Digital input indicators	Indicates presence of a voltage at the corresponding digital input pin (not necessarily a high logic level)
Digital output indicator	Indicates relay state
Counter input indicators	Indicates corresponding counter activity

Data memory

Table 13. Data memory

Parameter	Specification
Supported removable media	Secure Digital, Secure Digital High Capacity
Data file format	Binary. Data time stamped using real time clock.

Power

Table 14. Power specifications

Parameter	Condition	Specification
External power input		PWR+ (pin73) PWR– (pin74) 9 VDC min to 30 VDC max
External power supply		9 VDC to 30 VDC
Power supply fuse	0157002.DRT. - Littelfuse 2 A NANO$^{2®}$ Slo-Blo® Subminiature surface mount fuse	
Power supply current	+9 VDC input, continuous logging mode	LGR-5325: 225 mA typ, 630 mA max LGR-5327: 405 mA typ, 655 mA max LGR-5329:450 mA typ, 690 mA max
	+30 VDC input, continuous logging mode	LGR-5325: 100 mA typ, 210 mA max LGR-5327: 165 mA typ, 220 mA max LGR-5329: 175 mA typ, 230 mA max
Encoder supply (LGR-5327/5329 only)	External supply of 1.5 A @ 5 VDC fused up to 42.4 V_{pk} (50 V_{DC}) @ 2 A Protection diodes (30BQ060, 0.5 V_{max} drop) protecting against reverse polarity.	
Encoder supply fuse (LGR-5327/5329 only)	0157002.DRT. - Littelfuse 2 A NANO$^{2®}$ Slo-Blo® Subminiature Surface Mount Fuse	
Battery power	One 3 V button cell lithium battery (BR2032 or CR2032) required to power real-time clock when device is powered off.	

Note 7: The LGR-5325 AGND and GND pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.
The LGR-5327 AGND, GND and ENC- pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.
The LGR-5329 AGND, GND and ENC– pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) and the IGND (isolated ground) pins.

Chassis ground

Table 15. Chassis ground specifications

Parameter	Specification
Number of inputs	Single terminal EGND (pin 80)
Isolation method	10 nF/1000 V ceramic capacitor in parallel with 1 MΩ resistor

Note 8: The EGND pin is isolated from the measurement and I/O circuits. Only use the EGND pin to connect a LGR-5320 Series device to a local chassis ground connection. Do not use the EGND pin as a return path for any of the analog or digital I/O.

USB specifications

Table 16. USB specifications

Parameter	Specification
USB device type	USB 2.0 (full-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	3 meters max.
USB cable type	A-B cable, UL type AWM 2527 or equivalent

Environmental

Table 17. Environmental specifications

Parameter	Specification
Operating temperature range	0 to 55 °C
Storage temperature range	–40 to 85 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 18. Mechanical specifications

Parameter	Specification
Dimensions	9.5" L x 5.0" W x 1.75" H
Weight	505.85 g (1.12 lbs)
Mechanical shock (operating)	■ 50 g, 3 ms half sine ■ 30 g, 11 ms half sine Three hits per face for a total of 18 hits (18 hits at 50 g, 18 hits at 30 g Test procedure: IEC 60068-2-27
Random vibration (operating)	10 Hz to 500 Hz: 5 g_{rms} Test time: 100 minutes/axis Test procedure: IEC 60068-2-64

Screw terminal connector type

Table 19. Screw terminal connector specifications

Connector type	Detachable type
Wire gauge range	16 AWG to 30 AWG

LGR-5325 screw terminal pinout

Table 20. LGR-5325 8-channel differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0H	Channel 0 HI	96	AGND	Analog ground
2	AGND	Analog ground	95	CH7L	Channel 7 LO
3	CH0L	Channel 0 LO	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7H	Channel 7 HI
5	CH1H	Channel 1 HI	92	AGND	Analog ground
6	AGND	Analog ground	91	CH6L	Channel 6 LO
7	CH1L	Channel 1 LO	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6H	Channel 6 HI
9	CH2H	Channel 2 HI	88	AGND	Analog ground
10	AGND	Analog ground	87	CH5L	Channel 5 LO
11	CH2L	Channel 2 LO	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5H	Channel 5 HI
13	CH3H	Channel 3 HI	84	AGND	Analog ground
14	AGND	Analog ground	83	CH4L	Channel 4 LO
15	CH3L	Channel 3 LO	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4H	Channel 4 HI
17	RSVD	Reserved	80	EGND	Chassis ground
18	CTR0	Counter 0 input	79	AGND	Analog ground
19	RSVD	Reserved	78	ATRIG	Analog trigger input
20	UPDN0	Up/down 0 input	77	GND	Digital ground
21	RSVD	Reserved	76	DTRIG	Digital trigger
22	GATE0	Gate 0 input	75	PACER	Pacer I/O
23	RSVD	Reserved	74	PWR–	Input ground
24	GND	Digital ground	73	PWR+	Input power
25	RSVD	Reserved	72	NC	Relay normally closed contact
26	CTR1	Counter 1 input	71	COM	Relay common contact
27	RSVD	Reserved	70	NO	Relay normally open contact
28	UPDN1	Up/down 1 input	69	GND	Digital ground
29	RSVD	Reserved	68	RSVD	Reserved
30	GATE1	Gate 1 input	67	GND	Digital ground
31	RSVD	Reserved	66	GND	Digital ground
32	GND	Digital ground	65	GND	Digital ground
33	RSVD	Reserved	64	DIN15	Digital input 15
34	CTR2	Counter 2 input	63	DIN14	Digital input 14
35	RSVD	Reserved	62	DIN13	Digital input 13
36	UPDN2	Up/down 2 input	61	DIN12	Digital input 12
37	RSVD	Reserved	60	DIN11	Digital input 11
38	GATE2	Gate 2 input	59	DIN10	Digital input 10
39	RSVD	Reserved	58	DIN9	Digital input 9
40	GND	Digital ground	57	DIN8	Digital input 8
41	RSVD	Reserved	56	DIN7	Digital input 7
42	CTR3	Counter 3 input	55	DIN6	Digital input 6
43	RSVD	Reserved	54	DIN5	Digital input 5
44	UPDN3	Up/down 3 input	53	DIN4	Digital input 4
45	RSVD	Reserved	52	DIN3	Digital input 3
46	GATE3	Gate 3 input	51	DIN2	Digital input 2
47	RSVD	Reserved	50	DIN1	Digital input 1
48	GND	Digital ground	49	DIN0	Digital input 0

Table 21. LGR-5325 16-channel single-ended mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0	Channel 0	96	AGND	Analog ground
2	AGND	Analog ground	95	CH15	Channel 15
3	CH8	Channel 8	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7	Channel 7
5	CH1	Channel 1	92	AGND	Analog ground
6	AGND	Analog ground	91	CH14	Channel 14
7	CH9	Channel 9	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6	Channel 6
9	CH2	Channel 2	88	AGND	Analog ground
10	AGND	Analog ground	87	CH13	Channel 13
11	CH10	Channel 10	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5	Channel 5
13	CH3	Channel 3	84	AGND	Analog ground
14	AGND	Analog ground	83	CH12	Channel 12
15	CH11	Channel 11	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4	Channel 4
17	RSVD	Reserved	80	EGND	Chassis ground
18	CTR0	Counter 0 input	79	AGND	Analog ground
19	RSVD	Reserved	78	ATRIG	Analog trigger input
20	UPDN0	Up/down 0 input	77	GND	Digital ground
21	RSVD	Reserved	76	DTRIG	Digital trigger
22	GATE0	Gate 0 input	75	PACER	Pacer I/O
23	RSVD	Reserved	74	PWR–	Input ground
24	GND	Digital ground	73	PWR+	Input power
25	RSVD	Reserved	72	NC	Relay normally closed contact
26	CTR1	Counter 1 input	71	COM	Relay common contact
27	RSVD	Reserved	70	NO	Relay normally open contact
28	UPDN1	Up/down 1 input	69	GND	Digital ground
29	RSVD	Reserved	68	RSVD	Reserved
30	GATE1	Gate 1 input	67	GND	Digital ground
31	RSVD	Reserved	66	GND	Digital ground
32	GND	Digital ground	65	GND	Digital ground
33	RSVD	Reserved	64	DIN15	Digital input 15
34	CTR2	Counter 2 input	63	DIN14	Digital input 14
35	RSVD	Reserved	62	DIN13	Digital input 13
36	UPDN2	Up/down 2 input	61	DIN12	Digital input 12
37	RSVD	Reserved	60	DIN11	Digital input 11
38	GATE2	Gate 2 input	59	DIN10	Digital input 10
39	RSVD	Reserved	58	DIN9	Digital input 9
40	GND	Digital ground	57	DIN8	Digital input 8
41	RSVD	Reserved	56	DIN7	Digital input 7
42	CTR3	Counter 3 input	55	DIN6	Digital input 6
43	RSVD	Reserved	54	DIN5	Digital input 5
44	UPDN3	Up/down 3 input	53	DIN4	Digital input 4
45	RSVD	Reserved	52	DIN3	Digital input 3
46	GATE3	Gate 3 input	51	DIN2	Digital input 2
47	RSVD	Reserved	50	DIN1	Digital input 1
48	GND	Digital ground	49	DIN0	Digital input 0

LGR-5327/5329 screw terminal pinout

Table 22. LGR-5327/5329 8-channel differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0H	Channel 0 HI	96	AGND	Analog ground
2	AGND	Analog ground	95	CH7L	Channel 7 LO
3	CH0L	Channel 0 LO	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7H	Channel 7 HI
5	CH1H	Channel 1 HI	92	AGND	Analog ground
6	AGND	Analog ground	91	CH6L	Channel 6 LO
7	CH1L	Channel 1 LO	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6H	Channel 6 HI
9	CH2H	Channel 2 HI	88	AGND	Analog ground
10	AGND	Analog ground	87	CH5L	Channel 5 LO
11	CH2L	Channel 2 LO	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5H	Channel 5 HI
13	CH3H	Channel 3 HI	84	AGND	Analog ground
14	AGND	Analog ground	83	CH4L	Channel 4 LO
15	CH3L	Channel 3 LO	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4H	Channel 4 HI
17	ENC+	Encoder power output	80	EGND	Chassis ground
18	0PHA+	PHASE0A+ input	79	AGND	Analog ground
19	0PHA–	PHASE0A– input	78	ATRIG	Analog trigger input
20	0PHB+	PHASE0B+ input	77	GND	Digital ground
21	0PHB–	PHASE0B– input	76	DTRIG	Digital trigger
22	0IDX+	INDEX0+ input	75	PACER	Pacer I/O
23	0IDX–	INDEX0– input	74	PWR–	Input ground
24	ENC–	Encoder ground	73	PWR+	Input power
25	ENC+	Encoder power output	72	NC	Relay normally closed contact
26	1PHA+	PHASE1A+ input	71	COM	Relay common contact
27	1PHA–	PHASE1A– input	70	NO	Relay normally open contact
28	1PHB+	PHASE1B+ input	69	ENC–I	Encoder ground
29	1PHB–	PHASE1B– input	68	ENC+I	Encoder power input
30	1IDX+	INDEX1+ input	67	IGND (Note 9)	Isolated ground
31	1IDX–	INDEX1– input	66	IGND (Note 9)	Isolated ground
32	ENC–	Encoder ground	65	IGND (Note 9)	Isolated ground
33	ENC+	Encoder power output	64	DIN15	Digital input 15
34	2PHA+	PHASE2A+ input	63	DIN14	Digital input 14
35	2PHA–	PHASE2A– input	62	DIN13	Digital input 13
36	2PHB+	PHASE2B+ input	61	DIN12	Digital input 12
37	2PHB–	PHASE2B– input	60	DIN11	Digital input 11
38	2IDX+	INDEX2+ input	59	DIN10	Digital input 10
39	2IDX–	INDEX2– input	58	DIN9	Digital input 9
40	ENC–	Encoder ground	57	DIN8	Digital input 8
41	ENC+	Encoder power output	56	DIN7	Digital input 7
42	3PHA+	PHASE3A+ input	55	DIN6	Digital input 6
43	3PHA–	PHASE3A– input	54	DIN5	Digital input 5
44	3PHB+	PHASE3B+ input	53	DIN4	Digital input 4
45	3PHB–	PHASE3B– input	52	DIN3	Digital input 3
46	3IDX+	INDEX3+ input	51	DIN2	Digital input 2
47	3IDX–	INDEX3– input	50	DIN1	Digital input 1
48	ENC–	Encoder ground	49	DIN0	Digital input 0

Note 9: LGR-5329 only. Signal name is *GND* for *Digital ground* on the LGR-5327.

Table 23. LGR-5327/5329 16-channel single-ended mode pin out

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0	Channel 0	96	AGND	Analog ground
2	AGND	Analog ground	95	CH15	Channel 15
3	CH8	Channel 8	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7	Channel 7
5	CH1	Channel 1	92	AGND	Analog ground
6	AGND	Analog ground	91	CH14	Channel 14
7	CH9	Channel 9	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6	Channel 6
9	CH2	Channel 2	88	AGND	Analog ground
10	AGND	Analog ground	87	CH13	Channel 13
11	CH10	Channel 10	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5	Channel 5
13	CH3	Channel 3	84	AGND	Analog ground
14	AGND	Analog ground	83	CH12	Channel 12
15	CH11	Channel 11	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4	Channel 4
17	ENC+	Encoder power output	80	EGND	Chassis ground
18	0PHA+	PHASE0A+ input	79	AGND	Analog ground
19	0PHA–	PHASE0A– input	78	ATRIG	Analog trigger input
20	0PHB+	PHASE0B+ input	77	GND	Digital ground
21	0PHB–	PHASE0B– input	76	DTRIG	Digital trigger
22	0IDX+	INDEX0+ input	75	PACER	Pacer I/O
23	0IDX–	INDEX0– input	74	PWR–	Input ground
24	ENC–	Encoder ground	73	PWR+	Input power
25	ENC+	Encoder power output	72	NC	Relay normally closed contact
26	1PHA+	PHASE1A+ input	71	COM	Relay common contact
27	1PHA–	PHASE1A– input	70	NO	Relay normally open contact
28	1PHB+	PHASE1B+ input	69	ENC–I	Encoder ground
29	1PHB–	PHASE1B– input	68	ENC+I	Encoder power input
30	1IDX+	INDEX1+ input	67	IGND (Note10)	Isolated ground
31	1IDX–	INDEX1– input	66	IGND (Note10)	Isolated ground
32	ENC–	Encoder ground	65	IGND (Note10)	Isolated ground
33	ENC+	Encoder power output	64	DIN15	Digital input 15
34	2PHA+	PHASE2A+ input	63	DIN14	Digital input 14
35	2PHA–	PHASE2A– input	62	DIN13	Digital input 13
36	2PHB+	PHASE2B+ input	61	DIN12	Digital input 12
37	2PHB–	PHASE2B– input	60	DIN11	Digital input 11
38	2IDX+	INDEX2+ input	59	DIN10	Digital input 10
39	2IDX–	INDEX2– input	58	DIN9	Digital input 9
40	ENC–	Encoder ground	57	DIN8	Digital input 8
41	ENC+	Encoder power output	56	DIN7	Digital input 7
42	3PHA+	PHASE3A+ input	55	DIN6	Digital input 6
43	3PHA–	PHASE3A– input	54	DIN5	Digital input 5
44	3PHB+	PHASE3B+ input	53	DIN4	Digital input 4
45	3PHB–	PHASE3B– input	52	DIN3	Digital input 3
46	3IDX+	INDEX3+ input	51	DIN2	Digital input 2
47	3IDX–	INDEX3– input	50	DIN1	Digital input 1
48	ENC–	Encoder ground	49	DIN0	Digital input 0

Note 10: LGR-5329 only. Signal name *GND* for *Digital ground* on the LGR-5327.

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
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USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the products

LGR-5325, LGR-5327, LGR-5329

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- IEC 61000-4-4 (2004): Electric Fast Transient Burst Immunity.
- IEC 61000-4-5 (2001): Surge Immunity.
- IEC 61000-4-6 (2003): Radio Frequency Common Mode Immunity.
- IEC 61000-4-11 (2004): Voltage Interrupts.

To maintain compliance to the standards of this declaration, the following conditions must be met.

-
- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in October, 2009. Test records are outlined in Chomerics Test Report #EMI5475.09. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in April, 2010. Test records are outlined in Chomerics Test Report #TR5397.10.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

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